

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Leonard Forbes et al.

Title:

PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS

Docket No.:

1303.020US1

Serial No.: 09/943,134

Filed:

August 30, 2001

Due Date: N/A

Examiner:

Group Art Unit: 2818

Commissioner for Patents Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
 X An Information Divided A Communication
 X Copies of Co-Penal

X An Information Disclosure Statement (1 pg.), Form 1449 (3 pgs.), and copies of 41 cited references.

X A Communication Concerning Co-Pending Applications (2 pgs.).

 \underline{X} Copies of Co-Pending Applications (9 copies.).

RECEIVEL JUN 25 2002 TC 2800 MAIL ROOM

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

Atty: Edward J. Brooks, III

Reg. No. 40,925

<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this <u>17</u> day of June, 2002.

Gina M. Uphus

Signature

Name

Customer Number 21186

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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(GENERAL)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Serial No .: Leonard Forbes et al.

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PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH

ASYMMETRICAL TUNNEL BARRIERS

INFORMATION DISCLOSURE STATEMENT

sistant Commissioner for Patents Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTROP.

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Gina M. Uphus

Name

S/N 09/943,134

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Leonard Forbes et al. Applicant:

Serial No.:

09/943,134

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August 30, 2001

Examiner:

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PATENT

Group Art Unit: 2818

PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITHIL ROOM

ASYMMETRICAL TUNNEL BARRIERS

COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

imissioner for Patents Washington, D.C. 20231

Noted TH 11/18/02

Applicant would like to bring to the Examiner's attention the following related copending application(s) in the above-identified patent application:

Serial No. 10/028,001 Filing Date 12/20/2001

Attorney Docket 01303.035US1

Ly phom, Rest-mobiled

Title

PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL

BARRIERS

10/081,818

02/20/2002

01303.045US1

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ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW

ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS

01303.028US1 08/30/2001 09/945,554

Tom Drekey, lest. meilel

SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY **INSULATORS**

01303.024US1 08/30/2001 09/945,498 Lypham, Rest. Incital

DEAPROM WITH INSULATING METAL OXIDE INTERPOLY INSULATORS

09/945,512 08/30/2001 01303.027US1 Risa (3mp), Pol makel

IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING CO ENDING APPLIC

Serial Number: 09/943,134 Filing Date: August 30, 2001

Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS

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PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW 2002 TUNNEL BARRIER INTERPORTO MAIL ROOM INSULATORS

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FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

09/945,514 08/30/2001 01303.015US1 Victor Mandala, Rest. Non Final GRADED COMPOSITION GATE
INSULATORS TO REDUCE TUNNELING
BARRIERS IN FLASH MEMORY
DEVICES

09/945,395 08/30/2001 01303.019USI The Hur, no-hal

DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicant's Representatives,

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Cha an Impis

Signatur

Name